What is claimed is:

1. A system for generating forward error correction (FEC) packets, comprising:

a first FEC encoder that receives data and encodes first FEC data with the data to form FEC encoded data;

a second FEC encoder that encodes the FEC encoded data to produce second FEC data; and

an FEC packet formatter that formats the second FEC data into an FEC packet.

2. The system for generating FEC packets set forth in claim 1, wherein the FEC packet is inserted into an otherwise empty time division multiple access (TDMA) time slot.

3. The system for generating FEC packets set forth in claim 2, wherein a header associated with the data contains information associating the data with the second FEC data contained in the otherwise empty TDMA time slot.

4. The system for generating FEC packets set forth in claim 2, wherein a location corresponding to the otherwise empty TDMA time slot is predetermined by a TDMA master.

5. The system for generating FEC packets set forth in claim 1, further comprising:

a payload packet formatter that formats the FEC encoded data into a data packet.

6. The system for generating FEC packets set forth in claim 1, wherein the second FEC encoder employs a systematic block code to produce the second FEC data.

7. The system for generating FEC packets set forth in claim 1, wherein the FEC packet is ignored by a receiver to conserve power.

8. A system for decoding a forward error correction (FEC) packet, comprising:

a first FEC decoder that receives a data packet and an FEC packet and decodes data contained in the data packet using first FEC data contained in the FEC packet to produce partially decoded data; and

a second FEC decoder that receives the partially decoded data and further decodes the data based on second FEC data contained in the data packet.

9. The system for decoding the FEC packet set forth in claim 8, further comprising:

a header decoder to decode a header associated with the data packet and identify the FEC packet.

10. The system for decoding the FEC packet set forth in claim 8, wherein the FEC packet is received from a predetermined time division multiple access (TDMA) time slot.

11. The system for decoding the FEC packet set forth in claim 10, wherein a location corresponding to the TDMA time slot is predetermined by a transmitter.

12. The system for decoding the FEC packet set forth in claim 8, wherein the FEC packet is ignored by a receiver to conserve power.

13. A method of processing forward error correction (FEC) packets, comprising:

receiving a data packet that contains data and first FEC data;

receiving an FEC packet that contains second FEC data; and

deciding whether to use the second FEC data to process the data.

14. The method set forth in claim 13, comprising processing the data using second FEC data to produce partially decoded data.

15. The method set forth in claim 14, comprising processing the partially decoded data with first FEC data.

16. The method set forth in claim 15, wherein the recited acts are performed in the recited order.

17. The method set forth in claim 13, comprising processing the data using only the first FEC data.

18. The method set forth in claim 17, wherein the recited acts are performed in the recited order.

19. The method set forth in claim 13, comprising ignoring the second FEC data to conserve power.

20. The method set forth in claim 13, wherein the recited acts are performed in the recited order.